Experiment Report of Digital System

Logic Gate Design

**- Name: Han Yichen 韩一尘**

**- Student ID: 22722051**

**- Date: 2023/09/20**

## Aim

1. Design a comparator to compare two bits, the output will be 1 if two bits are equal;

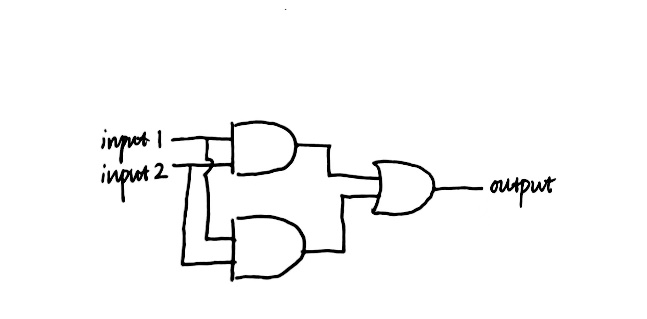
2. Design a two - out - of - three voter logic circuit using logic gates only. The circuit has 3 inputs (A, B and C) and 1 output. The output is 1 if two or more of the inputs are 1.

## Content and steps

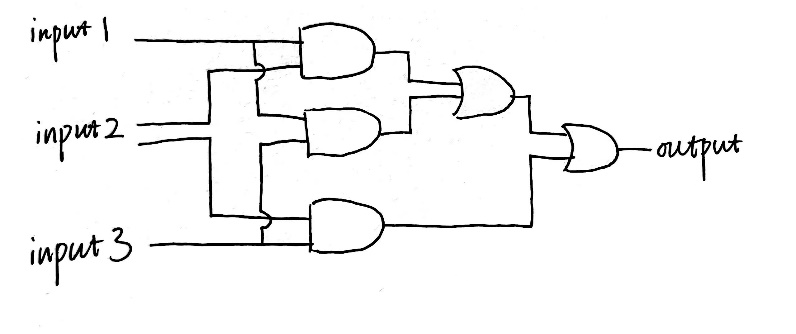
1. Draw a truth table and.
2. Write down the Boolean expression, and minimized Boolean expression by the way of the Karnaugh map.
3. Implement your minimized expression using logic gates only.
4. Draw the circuit.
5. Connect the circuit.
6. Verify the rationality of the circuit and the correctness of the truth table.

## Circuit

Experiment 1:

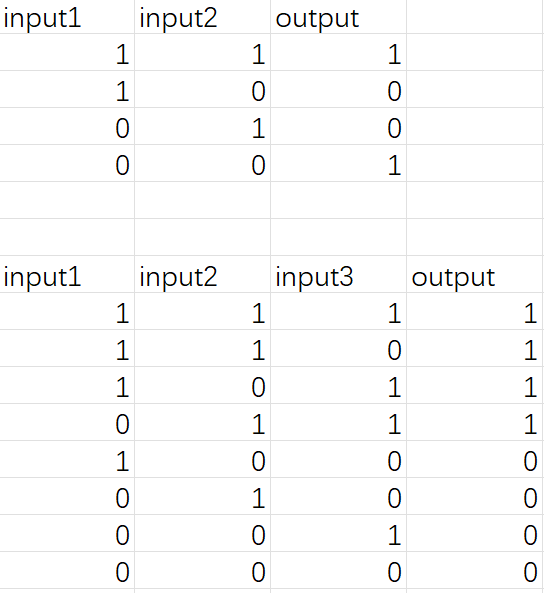


Experiment 2:



## Analysis

First, draw the truth table as shown:



Then, we can write and simplify the logical expressions as following:

So by the expression, we draw the circuits as the figures shown in the **Circuit** part and then connect the circuit as the figures shown in the **Result** part.

## Result

The connecting way of the circuit is shown as the following photograph (Experiment 1 is shown on the left, and Experiment 2 is shown on the right). For Experiment 1, when both inputs are high or low, the output value is high, otherwise it is low; For the second experiment, only when at least two inputs are high level, the output is high level, otherwise it is low level. This phenomenon is consistent with expectations, indicating that the experiment was successful.

